A New Four-level Dual Inverter fed Open-end Winding Induction Motor Drive

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Abstract - It is known that Four-level inversion can be achieved with two two-level inverters feeding an open-end winding induction motor from both ends with unequal DC link voltages in the ratio of 2:1. It is also known that this power circuit configuration could result in the overcharging of the DC-link capacitor corresponding to the inverter operating with the lower voltage. In this paper, a new power circuit topology is proposed, wherein, a rectifier-inverter combination is nested, or embedded, in the conventional two-level inverter configuration. The output of the conventional two-level inverter feeds one end of the open-end winding induction motor, while the output of the nested rectifier-inverter combination feeds the other end. By a judicious choice of the DC-link voltage of the embedded rectifier, it is possible to obtain a four-level drive, while avoiding the overcharging of the DC-link capacitor corresponding to the inverter operating with the lower DC input voltage. Also, the problem of zero-sequence currents, commonly encountered in Open-end winding induction motor drives, is avoided by resorting to a carrier based PWM scheme. This PWM scheme automatically ensures that the inverter connected to the higher DC-link voltage is switched with a lower frequency, compared to its low voltage counterpart.

I. INTRODUCTION

The dual-inverter fed open-end winding induction motor configuration offers an elegant alternative to the existing multilevel inverter configurations such as NPC, Flying capacitor and the cascaded H-bridge for induction motor drives [1]-[8]. One of the advantages of open-end winding configuration is that multilevel inversion is achieved by using the conventional two two-level inverters as a basic building block. A power circuit configuration to realize a four-level inverter with open-end winding induction motor, which employs two inverters with DC-link voltages in the ratio of 2:1 is reported in [4], is shown in Fig. 1. To suppress the zero-sequence components in the motor phases, each inverter is operated with an isolated DC power supply.

However, the space vector based PWM strategy proposed in [4] requires sector identification, making it cumbersome to implement. Also, it is plagued with the problem of overcharging of the capacitor of the inverter operating with a lower DC-link voltage. The phenomenon of overcharging of this capacitor and a possible solution for its avoidance, have been described in detail in [8].

This paper describes a new power circuit configuration, in which a rectifier-inverter combination is nested within the conventional two-level inverter configuration. The output the conventional two-level inverter feeds one end of the open-end winding induction motor, while the output of the nested rectifier-inverter combination feeds the other end.

In all, three isolated power supplies are needed in the proposed power circuit configuration, which are in the ratio – 1:2:1, their sum being equal to 2/3 of the sum of the voltages of the isolated power supplies needed in the scheme described in [4] (Fig. 1). This configuration avoids the overcharging of the DC-link capacitor corresponding to the inverter operating with the lower voltage. Also, the zero-sequence currents, commonly encountered in Open-end winding induction motor drives, are avoided by using a carrier based PWM scheme. This PWM scheme automatically ensures that the inverter connected to the higher DC-link voltage is switched with a lower frequency, compared to its low voltage counterpart.

In Fig. 1, Inverter-1 is operated with a DC-link voltage of \(2V_{dc}/3\), while inverter-2 is operated with a DC-link voltage of \(V_{dc}/3\). The space vectors offered by these two inverters are shown in Fig. 2. The combined effect of these two inverters is shown in Fig. 3, wherefrom it is evident that the power circuit shown in Fig. 1 is capable of rendering 4-level inversion. Combined 64(8*8) voltage space vectors are placed in 37 locations formed by 54 equilateral triangles of sides 1/3 \(V_{dc}\) is shown in Fig. 3.

In Fig. 2, a “+” means that the top switch of a leg is turned on, while “-” means that the bottom switch of the leg is turned on. The symbols \(V_{AO}, V_{BO}\) and \(V_{CO}\) denotes the pole voltages of inverter-1, while the symbols \(V_{AO'}, V_{BO'}\) and \(V_{CO'}\) denotes the same for inverter-2. The numbers 1 to 8 refer to the states assumed by inverter-1. Similarly the numbers 1’ to 8’ indicate the states assumed by inverter-2 (Fig. 2). Table-1 summarizes the values of the pole voltages of individual inverters. The difference of the pole voltages can thus attain one of the four possible values, which is the characteristic of a four level inverter.
From Fig. 4, it is evident that the capacitor of the inverter operating with a lower DC-link voltage could overcharge, disturbing the ratio of the DC-link voltages [8], which would result in the distortion of the motor phase voltages. The troublesome combinations [8], which could result in the overcharging of this capacitor, are shown in Fig. 5.

Table 1

<table>
<thead>
<tr>
<th>Pole-voltage of inverter-1 (V_{A1})</th>
<th>Pole-voltage of inverter-2 (V_{A2})</th>
<th>Motor phase voltage (V_{A})</th>
</tr>
</thead>
<tbody>
<tr>
<td>-V_{dc}/3</td>
<td>V_{dc}/6</td>
<td>-V_{dc}/2</td>
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<td>-V_{dc}/3</td>
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II. Effect of Space vector Combinations on DC-Link Capacitor of Individual Inverters

When it is intended to synthesize the reference vector \( \mathbf{O} \mathbf{A} \) (Fig. 3) located in sector 7, inverter-1 is clamped to state 1 and inverter-2 is switched amongst the states 8'-1'-6'-7'. Thus, the switching combinations 18', 11', 16' and 17' are deployed to construct the reference vector. The circuit situation corresponding to the deployment of the combination 11' is shown in Fig. 4.

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Fig. 2. Space vector locations of inverter-1 (Left) and inverter-2 (Right)

Fig. 3. Resultant space-vector combinations of the dual-inverter scheme

Fig. 4. Direction of charging currents for 11' combination

Fig. 5. Space-vector combinations which could over charge the DC link capacitor of the inverter with lower voltage

Fig. 6 and Fig. 7 depict the simulation and experimental results corresponding to the deployment of vector combinations, which overcharge this capacitor. (such as 11', 22', 12', 16'). Specifically, Fig. 6(a) shows the simulated motor phase voltage and Fig. 6(b) shows the experimentally obtained motor phase voltage when such combinations are used for a modulation index (m_a) of 0.4. The distortion in the motor phase voltage is evident. It may also be noted that there exists an appreciable congruence between the simulated and the experimental results.
In this work, the basic PWM technique, originally formulated for a two-level inverter in [9], is extended to suit the requirements of a four-level inverter. To this end, three triangular carrier waves are employed to compare the modulating wave output by the modulator. The modulating wave is obtained by resorting to the Space Vector Modulation scheme described in [9]. It is shown in [9] that the sine-triangle PWM technique is a specific case of a more generalized Space Vector Modulation. By simply varying a parameter called Offset-time, it is possible to implement sine-triangle PWM technique with a generalized implementation of SVPWM technique [9].

Fig. 10 (a) shows the simulated waveforms for the pole voltages of inverter-1 and inverter-2 (top and bottom traces respectively), for a modulation index of 0.4, with a centre spaced SVPWM. From these waveforms it is obvious that the inverter operated with a higher DC-link voltage is switched with a lower switching frequency compared to the one that operates with a higher switching frequency. The top trace of Fig. 10 (b) shows the motor phase voltage. It may be noted that the four levels of voltage shown in Table-1 are clearly visible. The bottom trace of Fig. 10(b) shows the motor phase current with a centre spaced SVPWM technique. With such a centre spaced PWM technique, the motor phase current shows the presence of zero-sequence currents as the motor phase voltage itself contains the zero-sequence component.

Fig. 12. D.C link voltages of inverter-1(left trace) and inverter-2(right trace) for ma=0.4.

IV. CONCLUSION

A new power circuit topology for 4-level inverter with an open-end winding drive is proposed in this paper, in which a rectifier-inverter is embedded within a conventional two-level inverter. The proposed circuit completely avoids the overheating of the capacitor of the inverter operating with a lower DC-link voltage. The carrier based PWM avoids the flow of zero-sequence currents, a nagging problem encountered in open-end induction motor drives. Also, the PWM scheme automatically ensures that the inverter operating with higher DC-link voltage is switched less frequently compared to its lower voltage counterpart.

REFERENCES