Analysis and Design of Zero-Voltage-Switching Current-Fed Isolated Full-Bridge Dc/Dc Converter

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Abstract—This paper presents steady-state analysis and design of current-fed full-bridge dc/dc converter with active-clamp. The converter utilizes the energy stored in the transformer leakage, aided by its magnetizing inductance to maintain zero-voltage-switching of H-bridge switches over wide range of input voltage and load variation. Active-clamp clamps the voltage across the switches at turn-off, allowing the selection and use of low voltage devices with low on-state resistance. In addition, this small and low rating active-clamp circuit results in zero-voltage transition circuit aiding in achieving zero voltage switching of the devices. All switches undergo soft turn-on and switching losses of the converter are reduced. It improves the converter efficiency and allows high switching frequency operation, which results in compact, light weight, and low cost system.

I. INTRODUCTION

Current-fed converters are picking-up attention in applications requiring higher voltage conversion ratio and which are sensitive to input current ripple. Also, it has been observed that for high-frequency (HF) switching operation, current-fed topologies can provide wide range soft-switching while maintaining higher efficiency compared to voltage-fed PWM and resonant converters for input voltage variation of 1:2 conditioning power from full load down to light load [1]. Current-fed topologies have been justified for fuel cells applications [2-3]. Low ripple current magnitude results operating point stability as well as fuel saving to enhance the overall system efficiency and to reduce the energy cost. In case of PV, the same results in better PV power utilization, stable MPPT, and possibly low payback period. Current-fed full bridge converter has been analyzed in [3-8].

Currently, current-fed converter topologies are cited in literature rapidly with the global boom in renewable energy market with concept of clean and green energy including transportation to save the environment, specially fuel cells applications, i.e., fuel cell inverter, electrolyser, fuel cell vehicles (FCV) etc. FCVs are on road in countries USA, Canada and Germany, not only cars but local transportation system as they have environmental impact due to zero emission. Similarly for PV micro-inverters, current-fed is a potential candidate among choices to utilize PV power efficiently over wide bandwidth of voltage and current with varying solar insolation and temperature.

Mostly, the literature on current-fed full-bridge topology is on hard-switching. Literature on active-clamp based [4-5, 9-13] ZVS current-fed full-bridge topology is limited. In this paper, authors do not claim on the topology. The topology has been discussed in [4-5]. However, the analysis and design presented are new and never reported in literature.

The objectives of this paper are to present the analysis and design of the high-frequency isolated active-clamped current-fed full-bridge dc/dc converter. The paper is organized as follow: Steady-state operation and analysis of the converter are described in Section II. Converter design procedure with a design example is illustrated in Section III. Simulation results to verify the analysis and design are presented in Section IV. Experimental results are presented in Section V.

II. OPERATION AND ANALYSIS OF THE CONVERTER

The following assumptions are made for the operation and analysis of the converter: 1) Input inductor \( L \) is large so that the current through it is considered constant. 2) Clamp capacitor \( C_o \) is large to maintain constant voltage across it. 3) All components including switches and diodes are ideal.

Steady-state operating waveforms are shown in Fig. 2. Switches \( S_i \) and \( S_o \) are operated by identical gating signals, and \( S_2 \) and \( S_3 \) are operated by same gating signals. Switching frequency of auxiliary switch \( S_{aux} \) is double of that of main switches. It is controlled by gating signal complementary to the main switches’ gating signals. Gating signals of switch pair \( S_2, S_3 \) are shifted in phase by 180° with gating signals of switch pair \( S_1, S_4 \) with an overlap. The overlap varies with duty cycle. Fixed frequency duty cycle modulation is used for control. The operation of the converter during different intervals in a HF half cycle is explained using the equivalent circuits shown in Fig. 3.

Fig. 1 Active-clamped ZVS current-fed full-bridge dc/dc converter.
Interval 1 (Fig. 3a; $t_0 < t < t_1$): In this interval, all four main switches $S_1 \sim S_4$ are ON. Auxiliary switch $S_{ax}$ is off. Input inductor $L$ is storing energy. Power is transferred to the load by the output filter capacitor $C_o$. Transformer magnetizing current circulates through its leakage inductance, given by

$$i_{lk} = i_{lk}' = -I_{mp}'$$  \hspace{1cm} (1)

where $i_{lk}$ is transformer input or leakage inductance current, $i_{lk}'$ is magnetizing current reflected to primary side and $I_{mp}'$ is the peak value of magnetizing current, given by

$$I_{mp}' = \frac{V_o}{2 \cdot f_s \cdot (L_{lk} + L_o')}. \hspace{1cm} (2)$$

Voltage across the auxiliary capacitor $C_a$ is

$$V_{Ca} = \frac{V_o}{2 \cdot (1 - D)}. \hspace{1cm} (3)$$

Voltage across the auxiliary switch is

$$V_{Sa} = V_{Ca} = \frac{V_o}{2 \cdot (1 - D)}. \hspace{1cm} (4)$$

Duty ratio of main switches $D = T_{on}/T_s$; $T_{on}$ = main switch conduction time and $T_s$ = switching period.

Interval 2 (Fig. 3b; $t_1 < t < t_2$): At $t = t_1$, main switches $S_2$ and $S_3$ are turned off. Input boost inductor $L_1$ current ($I_{in}$) diverts to the auxiliary circuit path causing zero current through all main switches. The magnetizing current flows through leakage inductance $L_{lk}$, anti-parallel diodes $D_1$, $D_4$ of main switches $S_1$ and $S_4$. Therefore, switch currents through $S_1$ and $S_4$ quickly dips to negative, which is equivalent to peak value of the reflected magnetizing current. Device capacitances $C_2$ and $C_3$ of main switches $S_2$ and $S_3$ start charging and auxiliary switch snubber capacitor $C_{ax}$ starts discharging linearly. Rectifier diodes are reverse biased and power is still transferred to the load by filter capacitor. The same constant current ($I_{mp}$) flows through magnetizing inductance. At the end of this interval, voltages across the main switch $S_2$ and auxiliary switch $S_{ax}$ reach $V_{S2}(t_2) = V_o/n$ and $V_{Sax}(t_2) = V_{Ca} + V_o/2$, respectively.

Interval 3 (Fig. 3c; $t_2 < t < t_3$): This interval is very small. Snubber capacitors, partially charged in interval 2, are still going through charging and discharging. The main switch voltages $V_{S2}$ and $V_{S3}$ increases from $V_o/n$ to $V_{Ca}$. A positive voltage equal to ($V_{Ca} - V_o/n$) appears across the transformer leakage inductance and current through it, $i_{lk}$ rises linearly. Output voltage $V_o$ appears across the magnetizing inductance $L_m$ and current through it starts increasing linearly. Rectifier diodes $DR_1$ and $DR_4$ are forward biased and start conducting when the leakage inductance current $i_{lk}$ rises above $I_{mp}'$ and power is transferred to the load. The leakage inductance current $i_{lk}$ is given by

$$i_{lk} = -I_{mp}' + \frac{V_o}{L_{lk}} \cdot \frac{V_o}{n} \cdot (t-t_2) \hspace{1cm} (5)$$

The magnetizing inductance current $I_{m}$ is given by

$$I_{m} = I_{mp}' + \frac{V_o}{L_{lk}} \cdot \frac{V_o}{n} \cdot (t-t_2) \hspace{1cm} (6)$$

$I_{mp}$ is the peak current through magnetizing inductance (on secondary side). Current through the switch $S_2$ is given by

$$i_{S2} = \frac{I_{m}}{2} - I_{mp}' + \frac{V_o}{L_{lk}} \cdot \frac{V_o}{n} \cdot (t-t_2) \hspace{1cm} (7)$$

The auxiliary clamp capacitor current $i_{Ca}$ decreases linearly.

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Fig. 2. Steady-state operating waveforms of current-fed full-bridge dc/dc converter with active-clamp.
At the end of this interval, the auxiliary switch snubber capacitor $C_{sa}$ is discharged completely to zero and $C_2$ and $C_3$ are charged to its full voltage, equal to $V_{Ca}$. Final values are: $v_{cas}(t_5) = v_{sat}(t_5) = 0$; $v_{s_2}(t_5) = v_{s_2}(t_5) = V_{Ca} = \frac{V_{Ca}}{2(1-D)}$.

**Interval 4** (Fig. 3d; $t_5 < t < t_6$): In this interval, the anti-parallel body diode $D_{ax}$ of the auxiliary switch $S_{ax}$ starts conducting and $S_{ax}$ can be gated for ZVS turn on. Leakage inductance current $i_k$ is increasing with the slope of $[(V_{Ca} - V_{o}/n)/L_{lk}]$. In this interval, switch current (through $S_1$ and $S_2$) changes direction to positive magnitude. Current through the magnetizing inductance is increasing with the same slope.

Transformer leakage inductance current $i_k$ is given by

$$i_k = i_{k1}(t_1) + \frac{V_{Ca} - (V_o/n)}{L_{lk}} \cdot (t - t_5) \quad (8)$$

Current through the switch $S_1$ is given by

$$i_{s_1} = i_{s_1}(t_1) + \frac{V_{Ca} - (V_o/n)}{L_{lk}} \cdot (t - t_5) \quad (9)$$

Magnetizing inductance current is given by

$$i_m = i_m(t_0) + \frac{V_o}{L_{mn}} \cdot (t - t_5) \quad (10)$$

Auxiliary capacitor current during this interval is decreasing and is given by

$$i_{ca} = i_{ca,peak} - \frac{V_o}{L_{mn}} \cdot (t - t_5) \quad (11)$$

At the end of this interval, i.e., $t = t_6$, $i_{ca}$ reaches zero, $i_k$ reaches $I_m$ and also switch current reaches $i_{s_1}$ reaches $I_m$. Final values are: $i_2(t_6) = I_m$; $i_{s_1}(t_6) = 0$; $i_{s_2}(t_6) = I_m$.

**Interval 5** (Fig. 3e; $t_6 < t < t_7$): In this interval, the auxiliary switch $S_{ax}$ is turned on with ZVS. Current $i_k$ increases above $I_m$ with the same slope as interval 4 and current $i_{ca}$ decreases linearly (negative direction). Current $i_m$ is increasing with the same slope as interval 4. The equations for this interval are

$$i_k = I_m + \left(\frac{V_{Ca} - V_o}{L_{lk}}\right) \cdot (t - t_6) \quad (12)$$

$$i_{s_1} = I_m + i_{ca} \quad (13)$$

$$i_{ca} = I_m - i_k = -\frac{(V_{Ca} - V_o)}{L_{mn}} \cdot (t - t_6) \quad (14)$$

Peak value of the switch current is given by

$$i_{s_{1,peak}} = I_m - I_{mp} + \frac{V_o}{f_c \cdot L_{mn}} \cdot (1 - D) \quad (15)$$

At the end of this interval, current $i_{ca}$ rises to negative peak $= I_m + I_{mp}$ and therefore the currents $i_k$ and $i_{s_1}$ reaches their peak value. Final values: $i_{ca}(t_7) = i_{ca,peak}$; $i_2(t_7) = I_{mp}$; $i_3(t_7) = I_{s_{1,peak}}$.

**Interval 6** (Fig. 3f; $t_7 < t < t_8$): The auxiliary switch $S_{ax}$ is turned off at $t = t_7$. Current $i_k$ charges $C_{ax}$ and discharges $C_2$ and $C_3$. The leakage inductance $L_{lk}$ resonates with snubber capacitors $C_{a1}$ and $C_2 + C_3$. This period is very short. and the series inductor current increases a very little in this interval.

The resonant frequency is given by

$$\omega_r = \frac{1}{\sqrt{L_{mn} \cdot (C_2 + C_3 + C_{a1})}} \quad (16)$$

Voltage across the capacitor $C_2$ or switch $S_2$ is given by

$$v_{s_2} = V_{Ca} - v_{sat} \quad (17)$$

where the voltage across the switch $S_{ax}$ (or capacitor $C_{ax}$) is given by

$$v_{sat} = I_{a,peak} \cdot \left(\frac{L_{mn}}{C_2 + C_3 + C_{a1}}\right) \cdot \sin(\omega_r \cdot (t - t_5)) \quad (18)$$

Main switch current is given by

$$i_s = I_{a,peak} \cdot \cos(\omega_r \cdot (t - t_5)) \quad (19)$$

At the end of this interval, $C_2$ and $C_3$ discharge to $V_{o}/n$ and $C_{ax}$ charges to $(V_{Ca} - V_{o}/n)$. Final values are (neglecting small increase in current in this short interval):

$$v_{cas}(t_9) = V_{Ca} - V_{o}/n; \quad v_{sat}(t_9) = V_{sat} / n$$

**Interval 7** (Fig. 3g; $t_7 < t < t_9$): Current $i_k$ is still charging $C_{ax}$ and discharging $C_2$ and $C_3$ in a resonant fashion. It is short time interval and the current $i_k$ decreases a very little in this interval. At the end of this interval, the capacitors $C_2$ and $C_3$ discharges completely to zero and capacitor $C_{ax}$ charges to its initial value. Final values are: $v_{sat}(t_9) = 0$; $v_{sat}(t_9) = V_{Ca}$.

**Interval 8** (Fig. 3h; $t_8 < t < t_9$): In this interval, anti-parallel body diode $D_2$ of main switch $S_2$ and $D_3$ of main switch $S_3$ start conducting and now $S_1$ and $S_2$ can be gated for ZVS turn on. Current $i_k$ decreases with a negative slope of $(V_{o}/nL_{mn})$.

$$i_k = I_k(t_7) - \frac{V_o}{n \cdot L_{mn}} \cdot (t - t_7) \quad (20)$$

$$i_{s_2} = i_k - I_m \quad (21)$$

This interval ends when current $i_k = I_m$. Final values are: $i_{s_2}(t_9) = 0$; $i_3(t_9) = I_m$.

**Interval 9** (Fig. 3i; $t_9 < t < t_{10}$): In this interval, switches $S_2$ and $S_1$ are turned on with ZVS. Currents $i_{s_2}$ and $i_{s_1}$ start increasing and the current $i_k$ is decreasing with the same slope. Current $i_k$ is transferred to the switches $S_2$ and $S_3$. The interval ends when current $i_k$ equals to the current $i_{s_1}$. Switch $S_2$ and $S_3$ current reaches to $I_{mp}$, $I_{mp}$ and $S_1$ and $S_4$ current reaches to $I_{mp}$.$I_{mp}$.

$$i_k = I_k(t_9) - \frac{V_o}{n \cdot L_{mn}} \cdot (t - t_9) \quad (22)$$

$$i_{s_2} = \frac{V_o}{n \cdot L_{mn}} \cdot (t - t_9) \quad (23)$$

$$i_{s_1} = I_m - \frac{V_o}{n \cdot L_{mn}} \cdot (t - t_9) \quad (24)$$

$$i_{s_4} = I_{mp} - I_{mp} \quad (25)$$

Final values: $i_{s_2}(t_9) = I_{mp}$, $i_{s_1}(t_9) = I_{mp}$, $i_{s_2}(t_9) = i_{s_4}(t_9)$.
The design procedure is illustrated by a design example with a converter of following specifications: Input voltage $V_m = 22$ to $41$ V, output voltage $V_o = 350$ V, output power $P_o = 1$ kW, switching frequency $f_s = 100$ kHz.

1. Average input current is $I_{in} = P_o/(\eta V_m)$. Assuming an efficiency $\eta$ of nearly 90%, $I_{in} = 50$ A.

2. $D_{max}$ is selected at minimum input voltage $V_{in} = 22$ V and full load based on switch voltage rating $V_{SW,max}$ using

$$D_{max} = 1 - \frac{V_{m}}{2 V_{SW,max}}$$

For $V_{SW(max)} = 55$ V, $D_{max} = 0.8$.

3. Values of boost inductor are given by

$$L = (V_{in})(D-0.5)/[(\Delta l_m)(f_s)]$$

where $\Delta l_m$ is the boost inductor ripple current. For $\Delta l_m = 1$ A, $L = 66$ $\mu$H. Maximum voltage across the inductors is $V_{Ca} = V_{in} = 33$ V.

4. Switch current ratings: Approximate value of rms current through the main switches $I_{S1,rms}$ can be given by

$$I_{S1,rms} = \left[ D \cdot \frac{I_{in}}{4} + I_{Ca} \right]^{1/2}$$

RMS current through the auxiliary switches is given by

$$I_{Sax,rms} = \left( I_{in} + I_{mp} \right) \left( l-1/2 \right)^{1/2}$$

The values of $I_{Sax,rms}$ and $I_{Sax,rms}$ are calculated to be 29.2 A and 7.1 A respectively.

Peak currents through main switches $I_{S1,peak} = 103$ A and auxiliary switches $I_{Sax,peak} = I_{in} + I_{mp,peak} = 55$ A.

Average current through auxiliary switches as well as anti-parallel diodes is given by

$$I_{Sax,av} = \left( I_{in} + I_{mp} \right) \left( l-1/2 \right) / 4$$

Here, $I_{S1,av} = 2.75$ A. Average current through the main switches $I_{S1,av} = I_{in}/2 = 25A$. 

For the next half cycle, the intervals are repeated in the same sequence with other symmetrical devices conducting to complete the full HF cycle. The analysis is done to obtain the design equations to design and select the components as well as to evaluate the converter’s performance theoretically.

Based on the above analysis, the design equations for the converter were derived and presented in the next section.

### III. DESIGN OF THE CONVERTER

In this section, design procedure is illustrated by a design example with a converter of following specifications: Input voltage $V_m = 22$ to $41$ V, output voltage $V_o = 350$ V, output power $P_o = 1$ kW, switching frequency $f_s = 100$ kHz.

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For $V_{SW(max)} = 55$ V, $D_{max} = 0.8$.

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For the next half cycle, the intervals are repeated in the same sequence with other symmetrical devices conducting to complete the full HF cycle. The analysis is done to obtain the design equations to design and select the components as well as to evaluate the converter’s performance theoretically.

Based on the above analysis, the design equations for the converter were derived and presented in the next section.
(5) Auxiliary capacitor: Substituting in (3), $V_{in} = 22$ V and $D = 0.8$, $V_{Ca} = 55$ V. The value of auxiliary capacitor $C_a$ is

$$C_a = \frac{I_{Ca,\text{peak}} \sqrt{2(1-D)/3}}{4 \pi f \cdot \Delta V_{Ca}}$$

(31)

Peak current through $C_a$ is $I_{Ca,\text{peak}} = I_{in} + I_{mp} = 55$ A. For a ripple voltage of $\Delta V_{Ca} = 2$ V, $C_a \approx 8$ mF.

RMS current through auxiliary capacitor is

$$I_{Ca,\text{rms}} = I_{Ca,\text{peak}} \sqrt{\frac{2}{3}(1-D)}$$

(32)

Here, $I_{Ca,\text{rms}} = 10.25$ A. Auxiliary capacitor carries a current of 200 kHz (twice the switching frequency).

(6) Output rectifier diodes: Average rectifier diode current is given by

$$I_{DR,\text{avg}} = \frac{P_o}{2V_o}$$

(33)

Here, $I_{DR,\text{avg}} \equiv 1.43$ A. Voltage rating of rectifier diodes, $V_{DR} = V_o = 350$ V.

(7) Output capacitor: Value of output filter capacitor $C_o$ is

$$C_o = \frac{\left(I_o - I_{T_o}\right) \cdot 2}{2 \cdot \Delta V_o}$$

(34)

$\Delta V_o = $ Allowable ripple in output voltage. $C_o = 10$ mF for $\Delta V_o = 0.72$ V. Its voltage rating is $V_o = 350$ V.

(8) Snubber design: The equation for the calculation of snubber capacitors is given by

$$(C_1 + C_4 + C_{sn}) = \frac{2 \cdot t_f \cdot (I_{in} + I_{mp}')(1-D)}{V_{in}}$$

(35)

Here, $t_f$ = fall time of the switches during turn-off. $C_1 = C_4 = C_{out, S2}$; $C_{sn} = (C_1 + C_4 + C_{a1}) - 2C_{out, S1}$. Here, $C_{out, S1}$ is the device capacitance of the selected main switches, which can be checked from their datasheet, then using (35), snubber capacitor $C_{sn}$ can be calculated.

IV. SIMULATION RESULTS

The designed converter has been simulated using software package PSIM 9.0. Simulation results are illustrated in Figs. 4-8. Figs. 4-8 coincide well with the theoretically predicted waveforms. It verifies the steady-state analysis of the converter, presented in Section II.

Fig. 4 shows the switch current waveforms through $S_1$ and $S_2$. The current through $S_1$ is identical to current through $S_2$ and current through $S_3$ is similar to current through $S_1$. It is clear from Fig. 4 that the anti-parallel body diode of the switch conducts before the starts conducting current through it. It results in ZVS on of the switches. It verifies the design of the converter explained in Section III.

Fig. 5 shows current waveforms through leakage and magnetizing inductances of the high-frequency transformer. Magnetizing inductance current follows the trapezoidal profile and leakage inductance current follows triangular profile. Their currents are identical reflected current whenever rectifier diodes are off, which is positive and negative peak of the magnetizing current. Average leakage inductance current is a measure of power transferred to the output. It is clear that its value is higher than 2$I_{in}$ as derived in the analysis Section of the converter.

Fig. 6 shows the waveforms of currents through auxiliary switch $S_{ax}$ and clamp capacitor $C_a$. Their frequency of operation is 200 kHz, i.e. twice of the main switches. Similar to main switches, the anti-parallel diode of the auxiliary switch conducts prior to conduction of the switch favoring its ZVS. Therefore, all the switches, main and auxiliary, are undergoing ZVS soft-switching. Their peak values are the sum of input current and reflected peak magnetizing current.

Fig. 7 shows the voltage waveforms across the leakage and magnetizing inductance of the high-frequency transformer. It is clear that the voltage across the magnetizing inductance is the output voltage and appears whenever the rectifier diodes are conducting. Due to capacitive output filter, it is free from duty cycle loss, voltage ringing and secondary snubber requirements. Voltage across the leakage inductance is very low. Low voltage results in low VA rating of the transformer.

Fig. 4. Switch current waveforms of current-fed full-bridge dc/dc converter with active-clamp.

Fig. 5. Transformer leakage and magnetizing inductance current waveforms of current-fed full-bridge dc/dc converter with active-clamp.
Fig. 8 illustrates the voltage across the main and auxiliary switches. The voltage across them is clamped at low voltage. The problem of high voltage stress, i.e., large turn-off voltage spike is eliminated. Low voltage switches can be used, which have low on-state resistance. Therefore, low conduction losses and high efficiency are expected.

V. EXPERIMENTAL RESULTS

A laboratory prototype of the current-fed isolated full bridge dc/dc converter rated at 500 W as shown in Fig. 9 was built in and tested to demonstrate the experimental results to verify the analysis. The converter has been tested for input voltage $V_{in} = 22$ V, output voltage $V_o = 350$ V, output power $P_o = 500$ W, switching frequency $f_s = 100$ kHz. Transformer secondary to primary turns ratio $n = 8$, and leakage and magnetizing inductances are $L_{lk} = 0.5$ µH (referred to primary) and $L_m = 32$ mH (referred to secondary) respectively. Experimental results are illustrated in Figs. 10-13.

Figs. 10-12 clearly confirm ZVS of main and auxiliary switches. In voltage waveforms shown in Fig. 10, gating signals ($v_{gs}$) are applied to main switches after voltage across them ($v_{ds}$) reaches zero resulting in zero voltage turn-on. The same is true for auxiliary switch $S_a$ as shown in Fig. 11. The ZVS of main and auxiliary switches is also confirmed by Fig. 12 since anti-parallel diode (negative) is conducting before the switch starts conducting (positive). Current through the transformer leakage inductance $l_{lk}$ is shown in Fig. 13.

Fig. 9. Experimental laboratory prototype of 500 W current-fed full-bridge isolated dc/dc converter.
The current waveforms through the switches (H-bridge and auxiliary clamp) and the transformer current can be superimposed on the theoretically predicted steady state waveforms and the same obtained by simulation. It verifies the proposed analysis and design.

VI. SUMMARY AND CONCLUSION

Current-fed topologies are suitable for low voltage higher current applications. However, these topologies suffer from higher voltage stress across the power semiconductor devices. Active-clamp helps clamp the voltage across the devices and low voltage devices can be selected. It results in low conduction losses and higher efficiency. In addition, active-clamp provides a path to circulate the energy stored in transformer leakage inductance. The re-circulation of energy discharges the snubber capacitors across the switches before they are gated for tuning on. It results in ZVS on of switches. Soft-switching permits high switching frequency operation resulting in compact, low cost and light weight system.

Steady-state analysis and design of current-fed full-bridge dc/dc converter with active-clamp have been presented in this paper. Simulation results using PSIM 9.0 are presented to verify the analysis and design. Complete mode-by-mode analysis and waveforms have been reported, which has never been illustrated in literature. Experimental results on a low power lab prototype have been demonstrated to show soft-switching operation and low voltage stress across the devices.

The duty cycle of the main switches is always kept greater than 50% due to increased circulating current through the auxiliary devices. It results in unwanted conduction losses causing lower converter efficiency, particularly at partial load as the auxiliary circuit loss becomes competitive to the losses in main switches.

REFERENCES


